REMARKS

In view of the above amendments and following remarks, reconsideration and further examination are requested.

As expressed in the Response filed December 14, 2004, the present invention is aimed at preventing any reduction in reliability that may occur from flip-chip mounting of a semiconductor device having a plate bonded to a rear side of a chip.

It is generally the case that flip-chip mounting of a semiconductor chip onto a substrate presents a problem of reliability due to a difference in thermal expansibility between the substrate and the chip. More specifically, the problem is that heat generated by the semiconductor chip itself, or any change in ambient temperature, or both, may cause cracking of solder, or metals such as gold, connecting the chip and the substrate, and thereby a defective connection therebetween results. This problem is effectively solved by using a chip having a reduced thickness. This reduced chip thickness allows for the chip to flex more easily to reduce any stress acting on a connecting solder or gold, and thereby an improved reliability, in terms of packaging, against any temperature variation is realized.

The reduced chip thickness, however, presents another problem in terms of handling the chip due to reduced chip strength resulting from the chip's reduced thickness. This problem is effectively solved by a plate bonded to a rear side of the chip via an adhesive layer. However, it is important to select a thickness and elastic modulus of the adhesive layer such that flexibility of the chip is not detrimentally hindered. It is particularly important to select the thickness and elastic modulus of the adhesive layer in accordance with the thickness of the chip.

These features are believed to be adequately recited in the claims. In this regard, current independent claim 1 requires that **a bonding layer has a thickness of from 25μm to 200μm and an elastic modulus of elasticity of at most 10,000 MPa for a semiconductor element having a thickness of at most 100μm**. These limitations ensure high reliability of connection between the chip and a substrate, as is clear from Fig. 8 of the application.

Additionally, the present invention includes a filler, having a given particle diameter, in an adhesive forming the bonding layer. This filler makes it possible to control a thickness of the adhesive layer within the range of 25μm to 200μm. This feature is also believed to be adequately recited in the claims. In this regard, current independent claim 3 requires that **a bonding layer has a thickness**

of from 25μm to 200μm for a chip having a thickness of at most 100μm, and that the bonding layer contains a filler functioning as a spacer between the semiconductor element and the plate so as to provide the bonding layer with a predetermined thickness.

In the Office Action mailed March 1, 2005, the claims were rejected over various combinations of Tobita et al., Barton, Takano et al., Distefano et al., Inaba et al. and Shikata et al. Because currently amended claim 1 includes the subject matter of former claim 2, and currently amended claim 3 generally corresponds to former claim 3 rewritten in independent form, the references will be discussed as they pertain to the rejections of former claims 2 and 3. That is, the rejection of claim 2 as being unpatentable over Tobita et al., Barton and Takano et al., and the rejection of claim 3 as being unpatentable over Tobita et al., Barton and Distefano et al. will be discussed below.

Rejection of claim 1

Tobita et al. discloses a thermally conductive polymer composition having a high degree of thermal conductivity for effective dissipation of heat from an electronic device, and a thermally conductive sheet molded from the polymer composition.

In Fig. 1C, Tobita et al. shows a thermally conductive sheet disposed between a semiconductor element and a heat sink. In order to transfer heat generated in the semiconductor element from the semiconductor element to the heat sink, paragraph [0058] states, with regard to the thickness of the thermally conductive sheet,

> The thickness of the thermally conductive sheet is not limited, but is preferably from 50μm to 10mm, and more preferably, 200μm to 5mm. When the thickness is less than 50μm, the sheet is hard to manufacture and handle. When the thickness is more than 10mm, thermal resistance becomes great, which is undesirable.

Thus, Tobita et al. limits the thickness of the thermally conductive sheet by considering its thermal conductivity, and is aimed at a different object than that of the present invention, which is aimed at ensuring reliability of connection between a semiconductor chip and a substrate.

In paragraph [0058], Tobita et al. also states, with regard to reduction of stress, that use of a thermally conductive sheet of low hardness is desirable. However, Tobita et al. does not state anything about hardness and thickness of the sheet in relation to reduction of stress, nor is there any discussion about the modulus of elasticity of the sheet. Additionally, in Tobita et al. there is no discussion about a relationship between the above parameters and the thickness of the semiconductor element.

Barton discloses a hybrid infrared focal plane array having a readout IC chip 12 sandwiched between a substrate 11 and an infrared detection portion 13 (a substrate 14 having a detection layer 16 formed thereon). Barton limits a thickness of the readout IC chip 12 to 1 to 20 mils in order to reduce any inconvenience caused by a thermal mismatch between the readout IC chip and the infrared detection portion 13. However, Barton does not disclose an adhesive layer according to the present invention between the readout IC chip 12 and the infrared detection portion 13. Accordingly, Barton does not disclose a numerical relationship between the thickness of the readout IC chip 12 and the thickness and elastic modulus of an adhesive layer.

Takano et al. discloses a semiconductor package including a resin substrate 12, a semiconductor chip 14 mounted on the substrate 12, and a cover plate 16 covering the semiconductor chip 14. The cover plate 16 has a bonding portion (flange) bonded to the substrate 12 by an adhesive 17, and a resin 15 fills a gap between the substrate 12 and the semiconductor chip 14. According to Table 2, the adhesive 17 has a Young's modulus of 900 MPa and the resin 15 has a Young's modulus of 7,000 MPa. However, Takano et al. is concerned with overcoming any warpage of the resinous substrate resulting from mechanical stress when the cover plate is attached to the IC chip on the substrate. Accordingly, in Takano et al. there is no discussion of dispersion of stress occurring from deformation (flexing) of a thin semiconductor element across its thickness during a manufacturing process, nor is there discussion of the thickness of the semiconductor chip as discussed by the present application. Thus, Takano et al. does not disclose any relationship between the thickness of the chip and the thickness and elastic modulus of the adhesive layer, as recited in claim 1.

Because none of Tobita et al., Barton nor Takano et al. is concerned with the problem addressed by Applicants, and because claim 1 is commensurate in scope with this problem by requiring a quantitative relationship between the thickness of the semiconductor chip and the thickness and elastic modulus of the bonding layer, it is respectfully submitted that one having

ordinary skill in the art would not have arrived at the invention as recited in claim 1 by considering the teachings of Tobita et al., Barton and Takano et al.

Additionally, in response to the position expressed by the Examiner in section 9.A. on page 10 of the Office Action, please note that the preamble of claim 12 requires that the semiconductor device is "**to be** mounted" onto a circuit board, and thus, contrary to the position taken by the Examiner, whether or not semiconductor element 12 of Tobita et al. is bonded to plate 19 prior to the semiconductor element being connected to printed circuit board 11 is of patentable significance. Without the phrase "to be", the Examiner's position would be well taken. Accordingly, the Examiner is respectfully requested to reconsider this position.

Thus, claim 1 is allowable.

Rejection of claim 3

In accordance with section 9.C. on page 11 of the Office Action, claim 3 now requires that the filler **functions as a spacer between the semiconductor element and the plate so as to provide the bonding layer with a predetermined thickness**. Such a feature is lacking from the references relied upon by the Examiner, and accordingly, claim 3 is allowable.

Thus, claims 1, 3-7, 12 and 23-25 are allowable.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicants' undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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